Intel® 925X and 925XE Express Chipset Memory Configuration Guide

White Paper

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Revision History

Revision Number	Description	Revision Date
-001	• Initial public release	June 2004
-002	• Added Intel® EM64T Support Information	August 2004
-003	• Added Intel® 925XE Express chipset information	November 2004

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1 Overview

The Intel® 925X and 925XE Express chipset Memory Controller Hub (MCH) is Intel's first dual-channel DDR2 Memory Controller Hub with Intel® Flex Memory Technology. Intel has enhanced its memory architecture design to allow for maximum configuration flexibility while providing optimal performance when combined with DDR2-533 and an Intel® Pentium 4® processor in the Land Grid Array 775 (LGA775) package with 800 MHz front side bus.

Note: *Information pertaining only to the Intel® 925XE Express chipset Memory Controller Hub (MCH) features will be italicized in this document.*

For great workstation application flexibility, the Intel® 925X and 925XE Express chipset is specifically designed to support Intel® Extended Memory 64 Technology Φ (Intel® EM64T) enabling 64-bit memory addressability. Select versions of the Pentium 4 processor support Intel EM64T as an enhancement to Intel's IA-32 architecture on workstation platforms. This enhancement enables the processor to execute operating systems and applications written to take advantage of Intel EM64T. Further details on the 64-bit extension architecture and programming model can be found in the Intel® Extended Memory 64 Technology Software Developer Guide at http://developer.intel.com/technology/64bitextensions/.

> Φ Intel® Extended Memory 64 Technology (Intel® EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations. See www.intel.com/info/em64t for more information including details on which processors support EM64T or consult with your system vendor for more information.

This document details the 925X and 925XE Express chipset MCH memory configurations and organization. It is intended for a technical audience interested in learning about the simplified population rules introduced by Intel® Flex Memory Technology and the 925X and 925XE Express chipset MCH platform. This document will provide background regarding the supported memory technologies and configurations, and then discuss styles of memory organization and operation.

1.1 Memory Technology Supported

The 925X and 925XE Express chipset Memory Controller Hub (MCH) supports DDR2 ECC and non-ECC DIMMs and memory technologies in the following configurations

- DDR2-400 (PC3200), DDR2-533 (PC4300)

Table 1. Memory Technology Support

DRAM Technology	Smallest Increments (One SS DIMM)	Largest Increments (One DS DIMM)	Maximum Capacity (Four DS DIMMs)
256 Mb	128 MB	512 MB	2048 MB
512 Mb	256 MB	1024 MB	4096 MB
1 Gb	512 MB	2000 MB	8000 MB (Note 1)

NOTES:
1. This exceeds a 32-bit address limit of 4 GB. In a 32-bit system, only the first 4 GB of memory will be accessible.

1.2 Illegal Configurations

The following configurations are not valid with the 925X and 925XE Express chipset MCH:

- 64-Mb, 128-Mb, 2-Gb, and 4-Gb Memory Technologies for DDR2
- x4, x32 DIMMs
- Double-Sided x16 DIMMs
- Registered DIMMs
- DDR DIMMs

1.3 Valid Front Side Bus and Memory Speeds

Table 2. Valid Memory Configurations

FSB	DRAM Data Rate	DRAM Type	Single Channel Peak Bandwidth	Dual Channel Peak Bandwidth
800 MHz	400 MT/s	DDR2 - DRAM	3.2 GB/s	6.4 GB/s
800 MHz	533 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s

1.4 ECC Support

The 925X and 925XE Express chipset MCH **supports** single-bit Error Correcting Code (or Error Checking and Correcting) on the main memory interface. The MCH generates an 8-bit code for each 64-bit qword of memory.

1.5 Latency Support

The 925X and 925XE Express chipset MCH **supports** the following latency timings on the main memory interface.

Table 3. Memory Latency Configurations

DRAM Data Rate	tCL	tRCD	tRP	Units	Notes
400 MT/s	*3*	*3*	*3*	*tCK*	*925XE only (1)*
400 MT/s	4	4	4	tCK	
533 MT/s	*3*	*3*	*3*	*tCK*	*925XE only (1)*
533 MT/s	4	4	4	tCK	
533 MT/s	5	5	5	tCK	

NOTES: *VCCSM voltage must be 1.9 V nominal in order to support latency timings of 3-3-3 for 533 MT/s*

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2 Intel® 925X and 925XE Express Chipset Memory Organization and Operating Modes

The 925X and 925XE Express chipset MCH memory interface is designed with Flex Memory Technology where it can be configured to support single-channel or dual-channel DDR2 memory configurations.

Depending upon how the DIMMs are populated on each system memory channel, a number of different configurations can exist for DDR2:

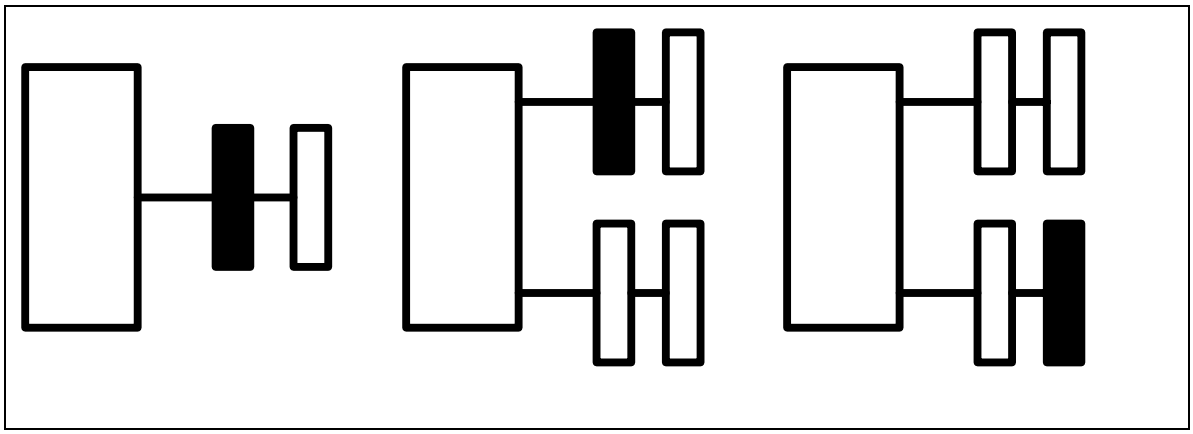
- Single Channel – only one channel of memory is routed and populated, or if two-channels of memory are routed, but only one channel is populated; can be either channel A or channel B.
- Dual Channel Asymmetric – both channels are populated, but each channel has a different amount (MB) of total memory.
- Dual Channel Symmetric – both channels are populated where each channel has the same amount (MB) of total memory.

The following sections explain and show the different memory configurations that are supported by the 925X and 925XE Express chipset.

2.1 Single-Channel

The system will enter single-channel mode when only one channel of memory is routed on the motherboard, or if two-channels of memory are routed, but only one channel is populated. In this configuration, all memory cycles are directed to a single channel.

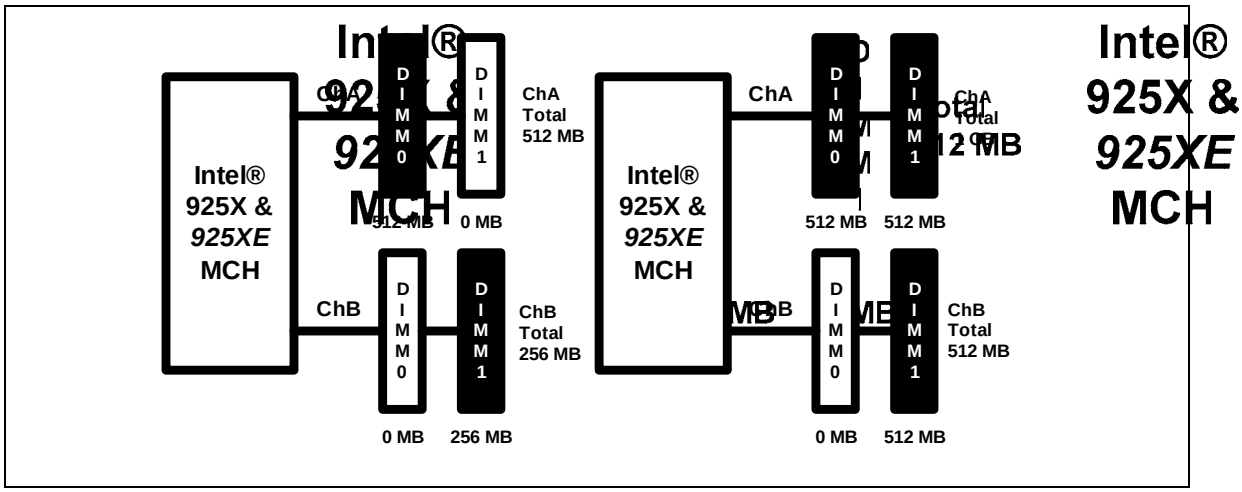
Figure 1. Single-Channel Memory Mode



2.2 Dual-Channel Asymmetric

This mode is entered when both memory channels are routed and populated with different amounts (MB) of total memory. This configuration allows addresses to be accessed in series across the channels starting in channel A until the end of its highest rank, then continue from the bottom of channel B to the top of the rank. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel.

Figure 2. Dual-Channel Asymmetric Memory Mode



2.3 Dual-Channel Symmetric

This mode allows the end user to achieve maximum performance on real applications by utilizing the full 64-bit dual-channel memory interface in parallel across the channels with the aid of Intel® Flex Memory Technology. The key advantage this technology brings is that the end user is only required to populate both channels with the same amount (MB) of total memory to achieve this mode. The DRAM component technology, device width, device ranks, and page size may vary from one channel to another.

Addresses are ping-ponged between the channels, and the switch happens after each cache line (64-byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels.

Figure 3. Dual-Channel Symmetric Memory Mode

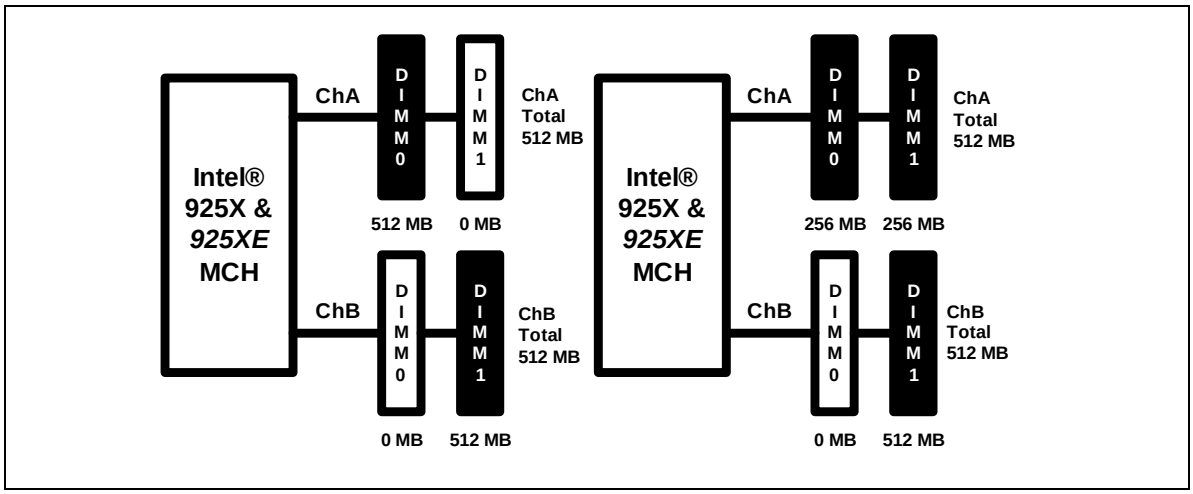
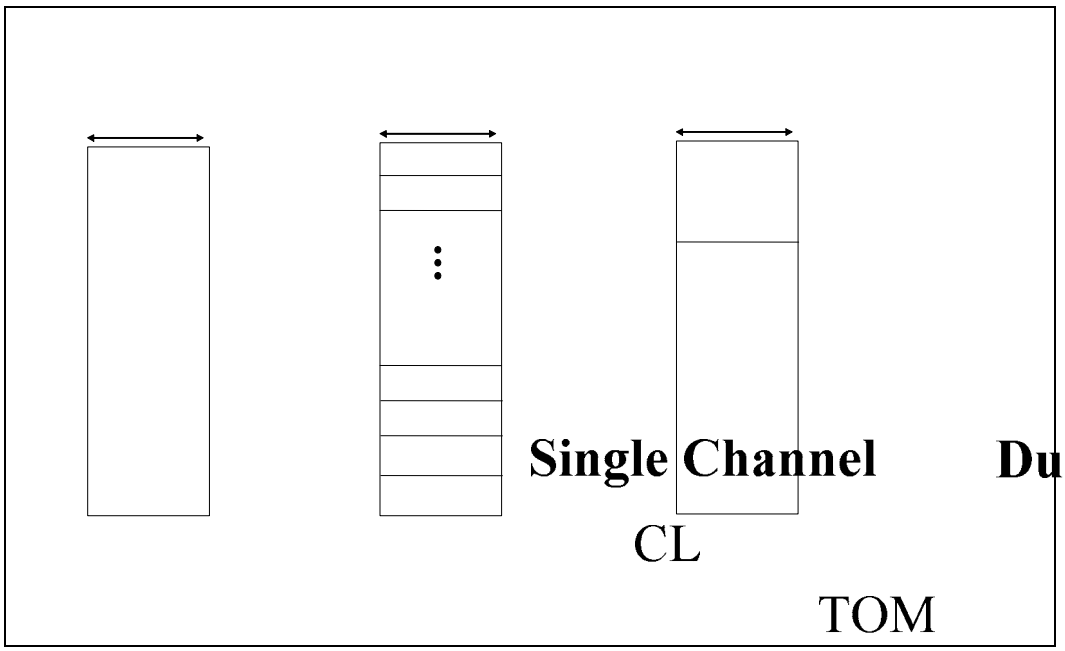


Figure 4. System Memory Mode Styles



2.4 Mixed DRAM Memory Speeds

The 925X and 925XE Express chipset MCH will accept mixed DDR2 speed populations, assuming the SPDs on the DIMMs are programmed with the correct information and the BIOS is programmed as outlined in Intel's BIOS reference code.

In all operating modes (Single-Channel, Dual Channel Asymmetric, and Dual-Channel Symmetric) the frequency of the System Memory will be set to the lowest frequency of all DIMMs populated in the system, as determined through the SPD registers on the DIMMs.

Example number one, a DDR2-533 DIMM installed with a DDR2-400 DIMM should run at 400 MHz. The DDR2-533 DIMM should downshift to DDR2-400 timings, thus allowing the system to run at 400 MHz speeds. The DDR2-533 DIMM will only downshift to DDR2-400, if the timings for DDR2-400 are programmed in the DDR2-533 DIMMs SPD.

Example number two, a DDR2-533 3-3-3 DIMM installed with a DDR2-533 4-4-4 DIMM should run at 533 MHz with 4-4-4 timings with VCCSM set at 1.8V nominal. The DDR2-533 3-3-3 DIMM should downshift to 4-4-4 timings and the VCCSM voltage on the platform should run at 1.8 V nominal.

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